



# 1.2 W fully differential audio power amplifier with selectable standby and 6 dB fixed gain

#### **Features**

- Differential inputs
- 90 dB PSRR @ 217 Hz with grounded inputs
- Operates from V<sub>CC</sub> = 2.5 V to 5.5 V
- 1.2 W rail-to-rail output power @ V<sub>CC</sub>=5 V, THD+N=1%, F=1 kHz, with an 8 Ω load
- 6 dB integrated fixed gain
- Ultra-low consumption in standby mode (10 nA)
- Selectable standby mode (active low or active high)
- Ultra-fast startup time: 10 ms typ. at V<sub>CC</sub>=3.3 V
- Available in 9-bump flip chip (300 mm bump diameter)
- Ultra-low pop and click

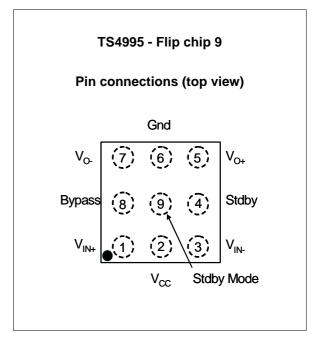
## **Applications**

- Mobile phones (cellular / cordless)
- PDAs
- Laptop / notebook computers
- Portable audio devices

# **Description**

The TS4995 is an audio power amplifier capable of delivering 1.2 W of continuous RMS output power into an 8  $\Omega$  load at 5 V. Thanks to its differential inputs, it exhibits outstanding noise immunity.

An external standby mode control reduces the supply current to less than 10 nA. A STBY MODE pin allows the standby pin to be active **high** or **low**. An internal thermal shutdown protection is also provided, making the device capable of sustaining short-circuits.



The TS4995 features an internal fixed gain at 6dB which reduces the number of external components on the application board.

The device is equipped with common mode feedback circuitry allowing outputs to be always biased at V<sub>CC</sub>/2 regardless of the input common mode voltage.

The TS4995 is specifically designed for high quality audio applications such as mobile phones and requires few external components.

Contents TS4995

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# 1 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
$V_{CC}$	Supply voltage (1)	6	V
V <sub>in</sub>	Input voltage (2)	GND to V <sub>CC</sub>	V
T <sub>oper</sub>	Operating free air temperature range	-40 to + 85	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C
Tj	Maximum junction temperature	150	°C
R <sub>thja</sub>	Thermal resistance junction to ambient (3)	200	°C/W
P <sub>diss</sub>	Power dissipation	Internally limited	W
ESD	MM: machine model (4)	200	V
LOD	HBM: human body model <sup>(5)</sup>	1.5	kV
Latch-up	Latch-up immunity	200	mA
-	Lead temperature (soldering, 10sec)	260	°C

- 1. All voltage values are measured with respect to the ground pin.
- 2. The magnitude of input signal must never exceed  $V_{CC}$  + 0.3 V / GND 0.3 V.
- 3. The device is protected in case of over temperature by a thermal shutdown activated at 150° C.
- Machine model: a 200 pF cap is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω), done for all couples of pin combinations with other pins floating.</li>
- 5. Human body model: 100 pF discharged through a 1.5  $k\Omega$  resistor between two pins of the device, done for all couples of pin combinations with other pins floating.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage	2.5 to 5.5	V
	Standby mode voltage input:		
V <sub>SM</sub>	Standby Active LOW Standby Active HIGH	V <sub>SM</sub> =GND V <sub>SM</sub> =V <sub>CC</sub>	V
	Standby voltage input:	SIVI CC	
V <sub>STBY</sub>	Device ON ( $V_{SM}$ =GND) or Device OFF ( $V_{SM}$ = $V_{CC}$ ) Device OFF ( $V_{SM}$ =GND) or Device ON ( $V_{SM}$ = $V_{CC}$ )	$1.5 \le V_{STBY} \le V_{CC}$ $GND \le V_{STBY} \le 0.4^{(1)}$	V
T <sub>SD</sub>	Thermal shutdown temperature	150	°C
R <sub>L</sub>	Load resistor	≥ 4	Ω
R <sub>thja</sub>	Thermal resistance junction to ambient	100	°C/W

The minimum current consumption (I<sub>STBY</sub>) is guaranteed when V<sub>STB Y</sub>= GND or V<sub>CC</sub> (the supply rails) for the whole temperature range.

# 2 Typical application schematics

Table 3. External component descriptions

Component	Component Functional description			
C <sub>s</sub>	Supply bypass capacitor that provides power supply filtering.			
C <sub>b</sub>	Bypass capacitor that provides half supply filtering.			
C <sub>in</sub>	Optional input capacitor that forms a high pass filter together with $R_{in}$ . $(F_{cl} = 1 / (2 \times \pi \times R_{in} \times C_{in})$			

Figure 1. Typical application

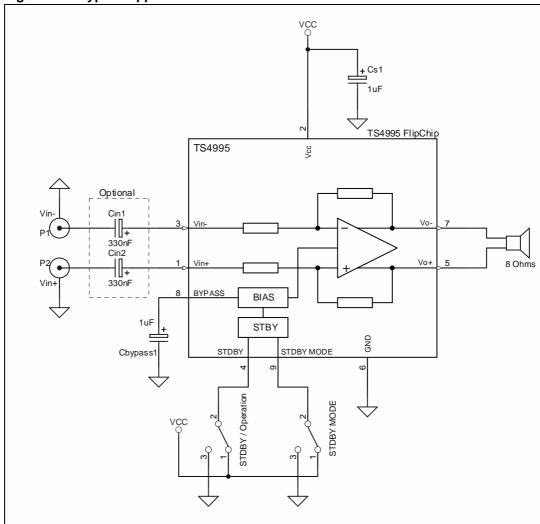


Table 4.  $V_{CC} = +5V$ , GND = 0V,  $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>CC</sub>	Supply current	No input signal, no load		4	7	mA
I <sub>STBY</sub>	Standby current	No input signal, $V_{STBY} = V_{SM} = GND$ , $R_L = 8\Omega$ No input signal, $V_{STBY} = V_{SM} = V_{CC}$ , $R_L = 8\Omega$		10	1000	nA
	Differential output offset voltage	No input signal, $R_L = 8\Omega$		0.1	10	mV
V <sub>IC</sub>	Input common mode voltage		0		4.5	V
Po	Output power	THD = 1% Max, F= 1kHz, $R_L = 8\Omega$	0.8	1.2		W
THD + N	Total harmonic distortion + noise	$P_0 = 850$ mW rms, $20$ Hz $\leq$ F $\leq$ $20$ kHz, $R_L = 8\Omega$		0.5		%
PSRR <sub>IG</sub>	Power supply rejection ratio with inputs grounded <sup>(1)</sup>	$F = 217Hz$ , $R = 8\Omega$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ripple} = 200 mV_{PP}$	75 <sup>(2)</sup>	90		dB
CMRR	Common mode rejection ratio	$F = 217Hz$ , $R_L = 8\Omega$ , $C_{in} = 4.7\mu F$ , $C_b = 1\mu F$ $V_{ic} = 200mV_{PP}$		60		dB
SNR	Signal-to-noise ratio	A-weighted filter $R_L = 8\Omega$ , THD +N < 0.7%, 20Hz $\leq$ F $\leq$ 20kHz		100		dB
GBP	Gain bandwidth product	$R_L = 8\Omega$		2		MHz
V <sub>N</sub>	Output voltage noise	$20$ Hz $\leq$ F $\leq$ $20$ kHz, R <sub>L</sub> = $8$ Ω Unweighted A-weighted Unweighted, standby A-weighted, standby		11 7 3.5 1.5		μV <sub>RMS</sub>
Z <sub>in</sub>	Input impedance		15	20	25	kΩ
-	Gain mismatch		5.5	6	6.5	dB
t <sub>WU</sub>	Wake-up time <sup>(3)</sup>	$C_b = 1 \mu F$		15		ms

 $<sup>1. \</sup>quad \text{Dynamic measurements - 20*log(rms(V_{out})/rms~(V_{ripple})).~V_{ripple}~is~the~super-imposed~sinus~signal~relative~to~V_{CC}.}$ 

<sup>2.</sup> Guaranteed by design and evaluation.

<sup>3.</sup> Transition time from standby mode to fully operational amplifier.

Table 5.  $V_{CC}$  = +3.3V (all electrical values are guaranteed with correlation measurements at 2.6V and 5V), GND = 0V,  $T_{amb}$  = 25°C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>CC</sub>	Supply current	No input signal, no load		3	7	mA
I <sub>STBY</sub>	Standby current	No input signal, $V_{STBY} = V_{SM} = GND$ , $R_L = 8\Omega$ No input signal, $V_{STBY} = V_{SM} = V_{CC}$ , $R_L = 8\Omega$		10	1000	nA
1 1/	Differential output offset voltage	No input signal, $R_L = 8\Omega$		0.1	10	mV
V <sub>IC</sub>	Input common mode voltage		0.4		2.3	V
Po	Output power	THD = 1% max, F= 1kHz, $R_L = 8\Omega$	300	500		mW
THD + N	Total harmonic distortion + noise	$P_0 = 300$ mW rms, $20$ Hz $\leq$ F $\leq$ $20$ kHz, $R_L = 8\Omega$		0.5		%
PSRR <sub>IG</sub>	Power supply rejection ratio with inputs grounded <sup>(1)</sup>	$F = 217Hz$ , $R = 8\Omega$ , $C_{in} = 4.7\mu F$ , $C_{b} = 1\mu F$ $V_{ripple} = 200mV_{PP}$	75 <sup>(2)</sup>	90		dB
CMRR	Common mode rejection ratio	$F = 217Hz$ , $R_L = 8Ω$ , $C_{in} = 4.7μF$ , $C_b = 1μF$ $V_{ic} = 200mV_{PP}$		60		dB
SNR	Signal-to-noise ratio	A-weighted filter $R_L = 8\Omega$ , THD +N < 0.7%, 20Hz $\leq$ F $\leq$ 20kHz		100		dB
GBP	Gain bandwidth product	$R_L = 8\Omega$		2		MHz
V <sub>N</sub>	Output voltage noise	<b>20Hz</b> $\leq$ <b>F</b> $\leq$ <b>20kHz</b> , <b>R</b> <sub>L</sub> = <b>8</b> Ω Unweighted A weighted Unweighted, standby A weighted, standby		11 7 3.5 1.5		μV <sub>RMS</sub>
Z <sub>in</sub>	Input impedance		15	20	25	kΩ
-	Gain mismatch		5.5	6	6.5	dB
t <sub>WU</sub>	Wake-up time <sup>(3)</sup>	C <sub>b</sub> =1µF		10		ms

 $<sup>1. \</sup>quad \text{Dynamic measurements - 20*log(rms(V_{out})/rms~(V_{ripple})).~V_{ripple}~is~the~super-imposed~sinus~signal~relative~to~V_{CC}.}$ 

<sup>2.</sup> Guaranteed by design and evaluation.

<sup>3.</sup> Transition time from standby mode to fully operational amplifier.

Table 6.  $V_{CC} = +2.6V$ , GND = 0V,  $T_{amb} = 25$ °C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>CC</sub>	Supply current	No input signal, no load		3	7	mA
I <sub>STBY</sub>	Standby current	No input signal, $V_{STBY} = V_{SM} = GND$ , $R_L = 8\Omega$ No input signal, $V_{STBY} = V_{SM} = V_{CC}$ , $R_L = 8\Omega$		10	1000	nA
V <sub>oo</sub>	Differential output offset voltage	No input signal, $R_L = 8\Omega$		0.1	10	mV
V <sub>IC</sub>	Input common mode voltage		0.6		1.5	V
Po	Output power	THD = 1% max, F= 1kHz, $R_L = 8\Omega$	200	300		mW
THD + N	Total harmonic distortion + noise	Po = 225mW rms, $20Hz \le F \le 20kHz$ , $R_L = 8\Omega$		0.5		%
PSRR <sub>IG</sub>	Power supply rejection ratio with inputs grounded <sup>(1)</sup>	F = 217Hz, R = 8 $\Omega$ , C <sub>in</sub> = 4.7 $\mu$ F, C <sub>b</sub> =1 $\mu$ F V <sub>ripple</sub> = 200mV <sub>PP</sub>	75 <sup>(2)</sup>	90		dB
CMRR	Common mode rejection ratio	$F=217Hz,R_L=8\Omega,\;\;C_{in}=4.7\mu\text{F},C_b=1\mu\text{F}$ $V_{ic}=200\text{mV}_{PP}$		60		dB
SNR	Signal-to-noise ratio	A-weighted filter $R_L = 8\Omega, \ THD + N < 0.7\%, \ 20Hz \le F \le 20kHz$		100		dB
GBP	Gain bandwidth product	$R_L = 8\Omega$		2		MHz
V <sub>N</sub>	Output voltage noise	20Hz ≤F ≤20kHz, R <sub>L</sub> = 8Ω  Unweighted A weighted Unweighted, standby A weighted, standby		11 7 3.5 1.5		μV <sub>RMS</sub>
Z <sub>in</sub>	Input impedance		15	20	25	kΩ
-	Gain mismatch		5.5	6	6.5	dB
t <sub>WU</sub>	Wake-up time <sup>(3)</sup>	C <sub>b</sub> =1µF		10		ms

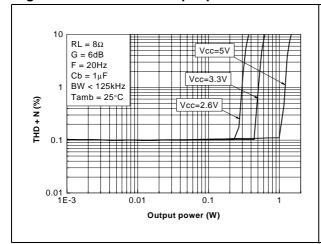
 $<sup>1. \</sup>quad \text{Dynamic measurements - } 20*log(\text{rms}(\text{V}_{\text{out}})\text{/rms }(\text{V}_{\text{ripple}})). \ \text{V}_{\text{ripple}} \ \text{is the super-imposed sinus signal relative to } \text{V}_{\text{CC}}.$ 

<sup>2.</sup> Guaranteed by design and evaluation.

<sup>3.</sup> Transition time from standby mode to fully operational amplifier.

Figure 2. THD+N vs. output power

Figure 3. THD+N vs. output power



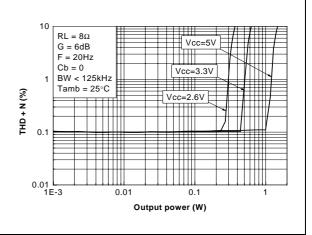
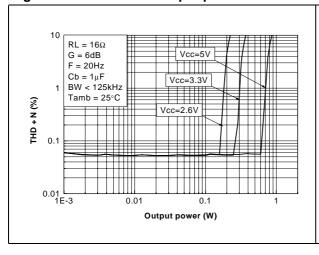


Figure 4. THD+N vs. output power

Figure 5. THD+N vs. output power



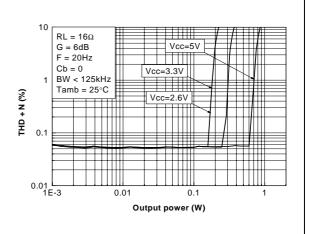
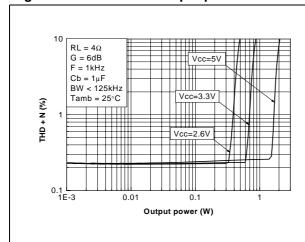


Figure 6. THD+N vs. output power

Figure 7. THD+N vs. output power



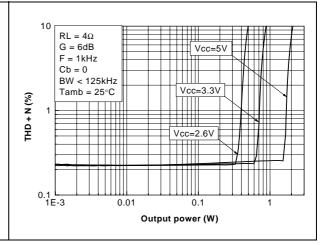
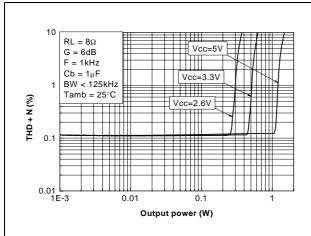


Figure 8. THD+N vs. output power

Figure 9. THD+N vs. output power



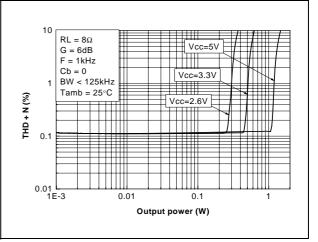
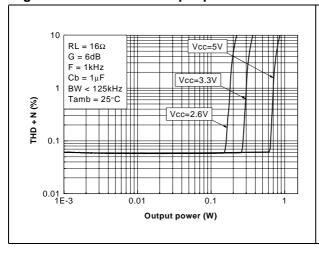


Figure 10. THD+N vs. output power

Figure 11. THD+N vs. output power



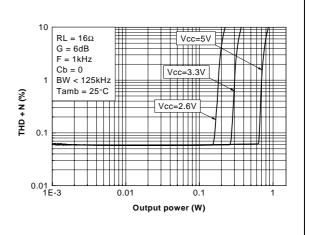
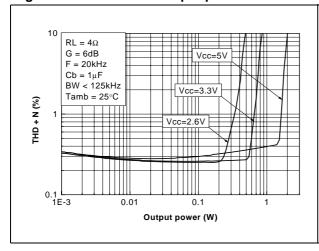


Figure 12. THD+N vs. output power

Figure 13. THD+N vs. output power



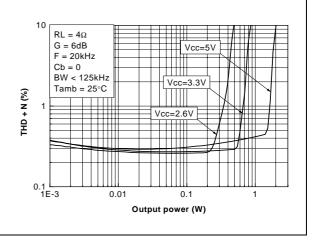
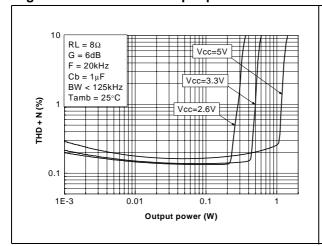


Figure 14. THD+N vs. output power

Figure 15. THD+N vs. output power



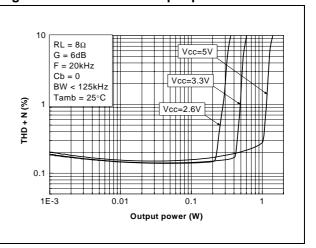
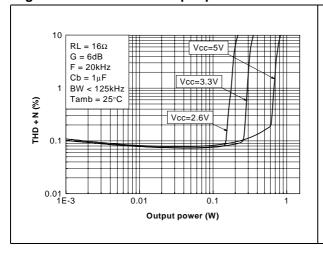


Figure 16. THD+N vs. output power

Figure 17. THD+N vs. output power



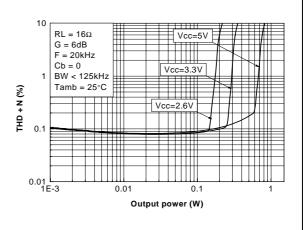
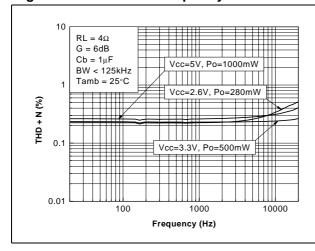


Figure 18. THD+N vs. frequency

Figure 19. THD+N vs. frequency



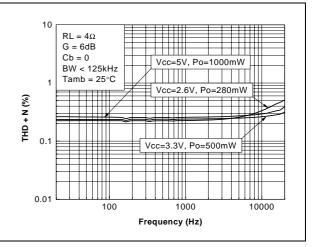


Figure 20. THD+N vs. frequency

10  $RL = 8\Omega$ G = 6dB $Cb = 1\mu F$ BW < 125kHz Tamb = 25C Vcc=2.6V, Po=225mW THD + N (%) Vcc=5V, Po=850mW 0.1 Vcc=3.3V, Po=300mW 0.01 100 1000 10000 Frequency (Hz)

Figure 21. THD+N vs. frequency

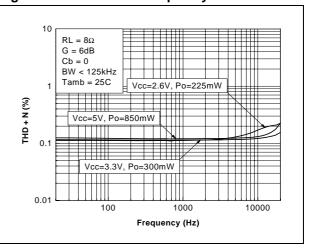


Figure 22. THD+N vs. frequency

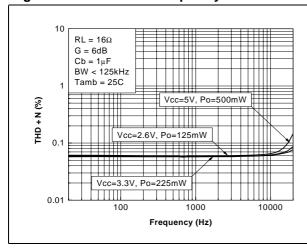


Figure 23. THD+N vs. frequency

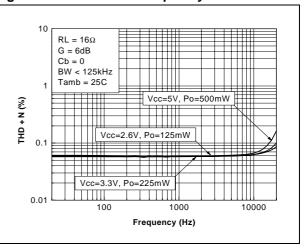


Figure 24. Output power vs. power supply voltage

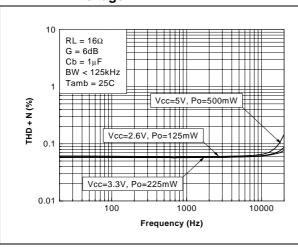


Figure 25. Output power vs. power supply voltage

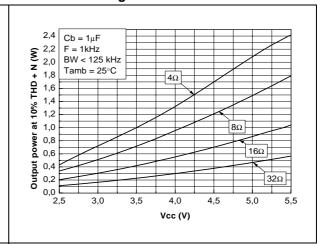
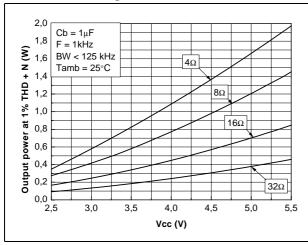


Figure 26. Output power vs. power supply voltage

Figure 27. Power derating curves



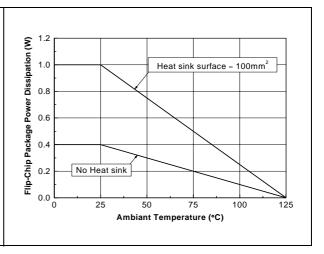
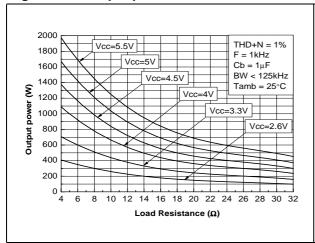


Figure 28. Output power vs. load resistance

Figure 29. Power dissipation vs. output power



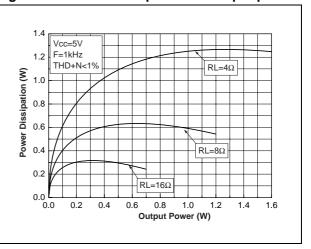
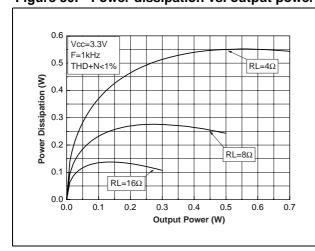
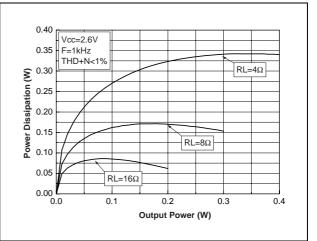


Figure 30. Power dissipation vs. output power Figure 31. Power dissipation vs. output power

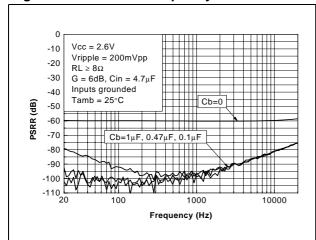




TS4995 Electrical characteristics

Figure 32. PSSR vs. frequency

Figure 33. PSSR vs. frequency



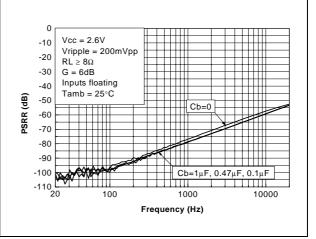
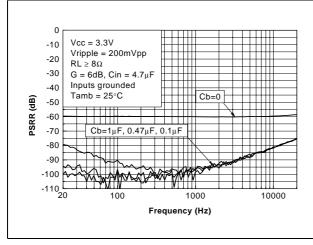


Figure 34. PSSR vs. frequency

Figure 35. PSSR vs. frequency



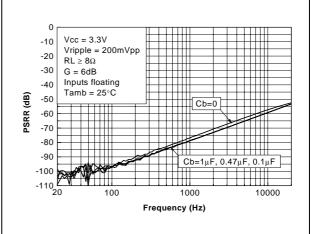
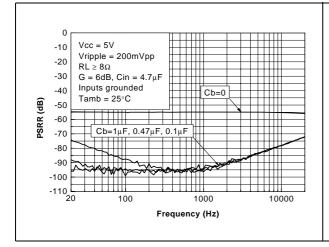


Figure 36. PSSR vs. frequency

Figure 37. PSSR vs. frequency



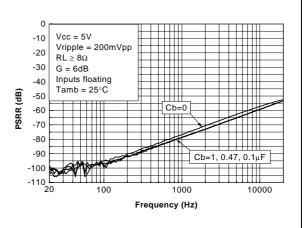
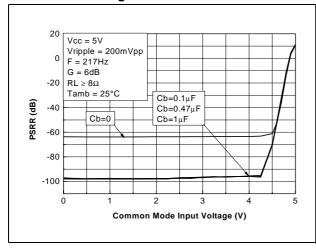


Figure 38. PSSR vs. common mode input voltage

Figure 39. PSSR vs. common mode input voltage



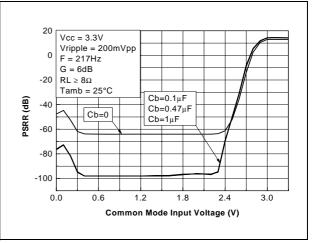
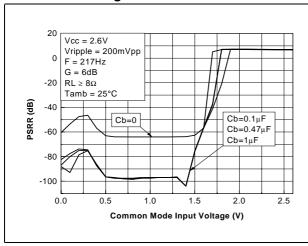


Figure 40. PSSR vs. common mode input voltage

Figure 41. CMRR vs. frequency



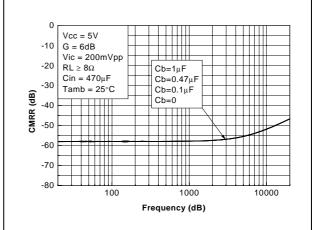
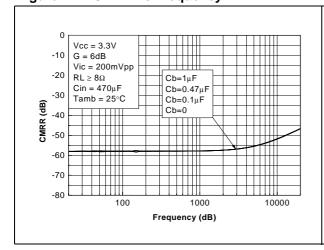


Figure 42. CMRR vs. frequency

Figure 43. CMRR vs. frequency



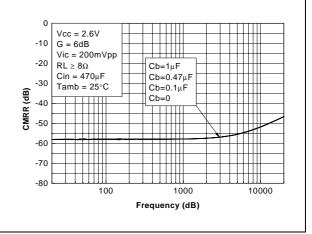


Figure 44. CMRR vs. common mode input voltage

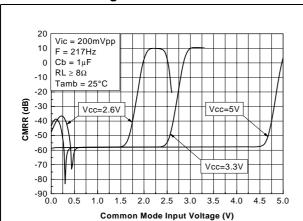


Figure 45. CMRR vs. common mode input voltage

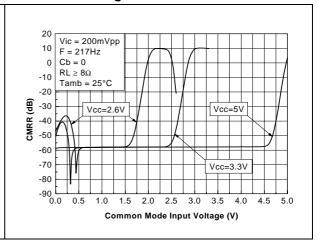


Figure 46. Current consumption vs. power supply voltage

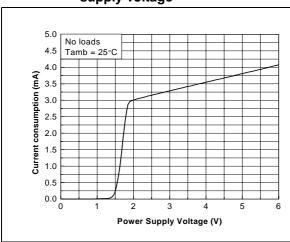
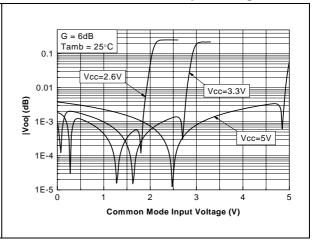


Figure 47. Differential DC output voltage vs. common mode input voltage



Current consumption vs. standby Figure 48. voltage

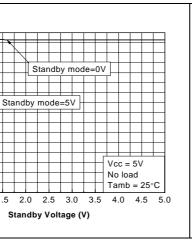
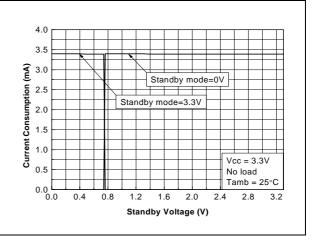


Figure 49. Current consumption vs. standby voltage



4.0

3.5

3.0

2.5

2.0 1.5

1.0

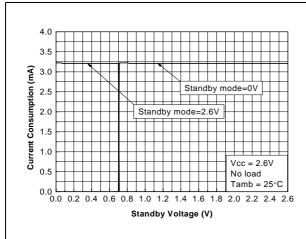
0.5

0.0 0.5 1.0

1.5

Current Consumption (mA)

Figure 50. Current consumption vs. standby Figure 51. Frequency response voltage



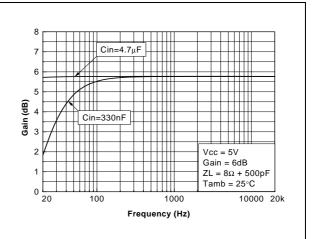


Figure 52. Frequency response

Cin=4.7μF 6 5 **(9** <sub>4</sub> Cin=330nF Gain 3 Vcc = 3.3VGain = 6dB  $ZL = 8\Omega + 500pF$  $Tamb = 25^{\circ}C$ 0 10000 20k 20 100 1000 Frequency (Hz)

Figure 53. Frequency response

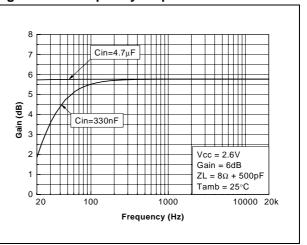
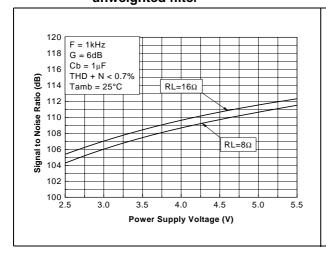
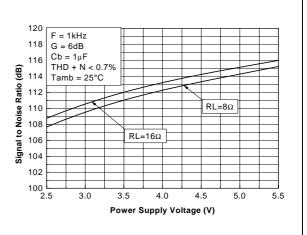


Figure 54. SNR vs. power supply voltage with Figure 55. SNR vs. power supply voltage with unweighted filter A-weighted filter





# 4 Application information

### 4.1 Differential configuration principle

The TS4995 is a monolithic full-differential input/ output power amplifier with fixed +6 dB gain. The TS4995 also includes a common mode feedback loop that controls the output bias value to average it at  $V_{\rm CC}/2$  for any DC common mode input voltage. This allows maximum output voltage swing, and therefore, to maximize the output power. Moreover, as the load is connected differentially instead of single-ended, output power is four times higher for the same power supply voltage.

The advantages of a full-differential amplifier are:

- Very high PSRR (power supply rejection ratio)
- High common mode noise rejection
- Virtually no pop and click without additional circuitry, giving a faster start-up time compared to conventional single-ended input amplifiers
- Easier interfacing with differential output audio DAC
- No input coupling capacitors required due to common mode feedback loop

In theory, the filtering of the internal bias by an external bypass capacitor is not necessary. However, to reach maximum performance in all tolerance situations, it is recommended to keep this option.

## 4.2 Common mode feedback loop limitations

As explained previously, the common mode feedback loop allows the output DC bias voltage to be averaged at  $V_{CC}/2$  for any DC common mode bias input voltage.

Due to the V<sub>IC</sub> limitation of the input stage (see *Table 4 on page 5*), the common mode feedback loop can fulfil its role only within the defined range.

# 4.3 Low frequency response

The input coupling capacitors block the DC part of the input signal at the amplifier inputs.  $C_{in}$  and  $R_{in}$  form a first-order high pass filter with -3 dB cut-off frequency.

$$F_{CL} = \frac{1}{2 \times \pi \times R_{in} \times C_{in}} \quad \text{(Hz)}$$

Note:

The input impedance for the TS4995 is typically  $20k\Omega$  and there is tolerance around this value

From Figure 56, you can easily establish the C<sub>in</sub> value required for a -3 dB cut-off frequency.

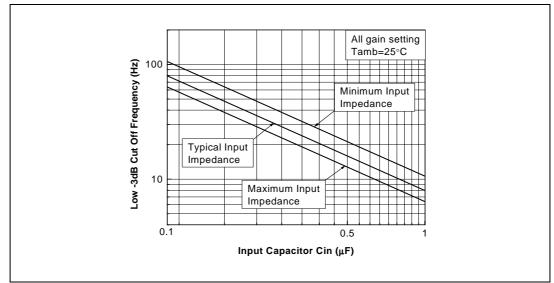


Figure 56. -3 dB lower cut-off frequency vs. input capacitance

# 4.4 Power dissipation and efficiency

#### **Assumptions:**

- Load voltage and current are sinusoidal (V<sub>out</sub> and I<sub>out</sub>)
- Supply voltage is a pure DC source (V<sub>CC</sub>)

The output voltage is:

$$V_{out} = V_{peak} \sin \omega t (V)$$

and

$$I_{out} = \frac{V_{out}}{R_L} (A)$$

and

$$P_{out} = \frac{V_{peak}^{2}}{2R_{L}} (W)$$

Therefore, the average current delivered by the supply voltage is:

#### **Equation 1**

$$Icc_{AVG} = 2 \frac{V_{peak}}{\pi R_L} (A)$$

The power delivered by the supply voltage is:

#### **Equation 2**

$$P_{\text{supply}} = V_{\text{CC}} I_{\text{ccAVG}} (W)$$

Therefore, the power dissipated by each amplifier is:

$$P_{diss} = P_{supply} - P_{out}(W)$$

$$P_{diss} = \frac{2\sqrt{2}V_{CC}}{\pi \sqrt{R_1}} \sqrt{P_{out}} - P_{out}$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{out}} = 0$$

and its value is:

#### **Equation 3**

$$Pdiss max = \frac{2 Vcc^2}{\pi^2 R_L} (W)$$

Note: This maximum value is only dependent on the power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply:

#### **Equation 4**

$$\eta = \frac{P_{out}}{P_{supply}} = \frac{\pi V_{peak}}{4 V_{CC}}$$

The maximum theoretical value is reached when  $V_{peak} = V_{CC}$ , so:

$$\eta = \frac{\pi}{4} = 78.5\%$$

The maximum die temperature allowable for the TS4995 is 125° C. However, in case of overheating, a thermal shutdown set to 150° C, puts the TS4995 in standby until the temperature of the die is reduced by about 5° C.

To calculate the maximum ambient temperature T<sub>amb</sub> allowable, you need to know:

- The power supply voltage, V<sub>CC</sub>
- The load resistor value, R<sub>I</sub>
- The package type, R<sub>thja</sub>

**Example:**  $V_{CC}$ =5 V,  $R_L$ =8  $\Omega$ ,  $R_{thja\text{-flipchip}}$ = 100° C/W (100 mm² copper heatsink).

Using the power dissipation formula given above in *Equation 3*, this gives a result of:

$$P_{dissmax} = 633 \text{mW}$$

T<sub>amb</sub> is calculated as follows:

#### **Equation 5**

$$T_{amb} = 125^{\circ} C - R_{thia} \times P_{dissmax}$$

Therefore, the maximum allowable value for T<sub>amb</sub> is:

$$T_{amb} = 125-100x0.633=61.7^{\circ} C$$

### 4.5 Decoupling of the circuit

Two capacitors are needed to correctly bypass the TS4995: a power supply bypass capacitor  $C_S$  and a bias voltage bypass capacitor  $C_b$ .

The  $C_S$  capacitor has particular influence on the THD+N at high frequencies (above 7 kHz) and an indirect influence on power supply disturbances. With a value for  $C_S$  of 1  $\mu$ F, one can expect THD+N performance similar to that shown in the datasheet.

In the high frequency region, if  $C_S$  is lower than 1  $\mu$ F, then THD+N increases and disturbances on the power supply rail are less filtered.

On the other hand, if  $C_S$  is greater than 1  $\mu F$ , then those disturbances on the power supply rail are more filtered.

The C<sub>b</sub> capacitor has an influence on the THD+N at lower frequencies, but also impacts PSRR performance (with grounded input and in the lower frequency region).

# 4.6 Wake-up time t<sub>WU</sub>

When the standby is released to put the device ON, the bypass capacitor  $C_b$  is not charged immediately. Because  $C_b$  is directly linked to the bias of the amplifier, the bias will not work properly until the  $C_b$  voltage is correct. The time to reach this voltage is called the wake-up time or  $t_{WU}$  and is specified in *Table 4 on page 5*, with  $C_b$ =1 µF. During the wake-up phase, the TS4995 gain is close to zero. After the wake-up time, the gain is released and set to its nominal value.

If  $C_b$  has a value different from 1  $\mu$ F, then refer to the graph in *Figure 57* to establish the corresponding wake-up time.

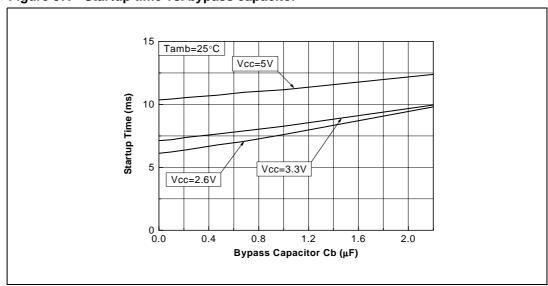


Figure 57. Startup time vs. bypass capacitor

### 4.7 Shutdown time

When the standby command is set, the time required to put the two output stages in high impedance and the internal circuitry in shutdown mode is a few microseconds.

Note:

In shutdown mode, the Bypass pin and  $V_{in}$ +,  $V_{in}$ - pins are shorted to ground by internal switches. This allows a quick discharge of  $C_b$  and  $C_{in}$ .

### 4.8 Pop performance

Due to its fully differential structure, the pop performance of the TS4995 is close to perfect. However, due to mismatching between internal resistors  $R_{\rm in}$ ,  $R_{\rm feed}$ , and external input capacitors  $C_{\rm in}$ , some noise might remain at startup. To eliminate the effect of mismatched components, the TS4995 includes pop reduction circuitry. With this circuitry, the TS4995 is close to zero pop for all possible common applications.

In addition, when the TS4995 is in standby mode, due to the high impedance output stage in this configuration, no pop is heard.

## 4.9 Single-ended input configuration

It is possible to use the TS4995 in a single-ended input configuration. However, input coupling capacitors are needed in this configuration. The schematic diagram in *Figure 58* shows an example of this configuration.

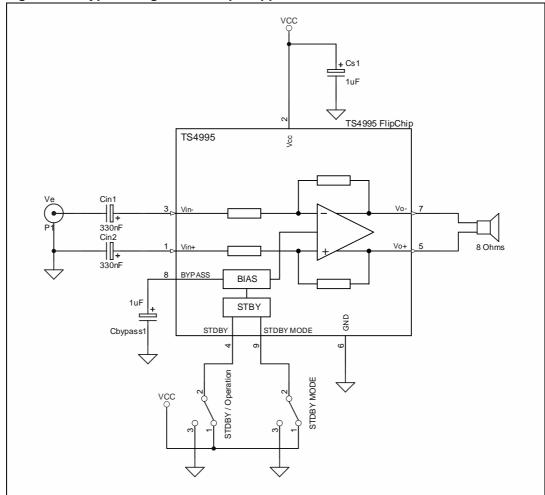


Figure 58. Typical single-ended input application

TS4995 Package information

# 5 Package information

To meet environmental requirements, STMicroelectronics offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: <a href="https://www.st.com">www.st.com</a>.

Figure 59. 9-bump flip-chip package mechanical drawing

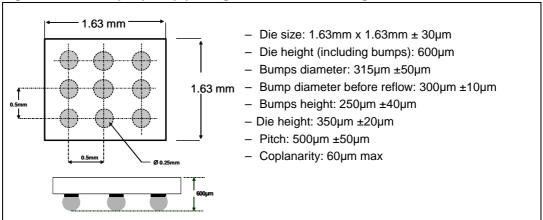
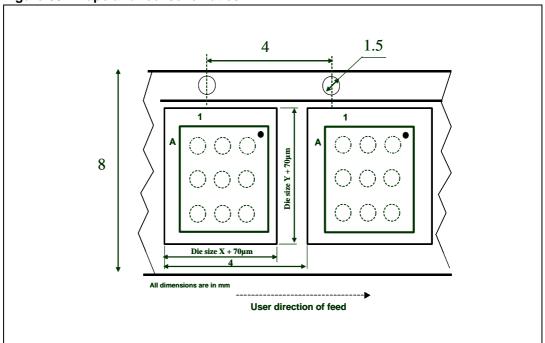


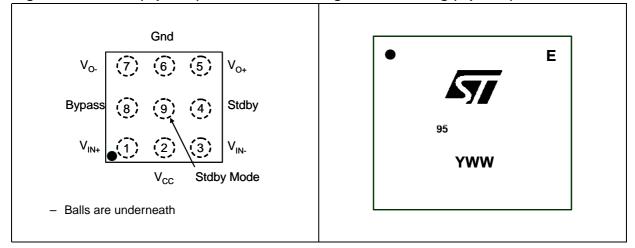
Figure 60. Tape and reel schematics



Package information TS4995

Figure 61. Pin out (top view)

Figure 62. Marking (top view)



TS4995 Ordering information

# 6 Ordering information

Table 7. Order code

Order code	Temperature range	· Package		Marking
TS4995EIJT	-40° C to +85° C	Lead free flip chip 9	Tape & reel	95

# 7 Revision history

Table 8. Document revision history

Date	Revision	Changes
1-Jun-2006	1	Final datasheet.
25-Oct-2006	2	Additional information for $4\Omega$ load.
25-Mar-2008 3		Modified Figure 60: Tape and reel schematics to correct die orientation.

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